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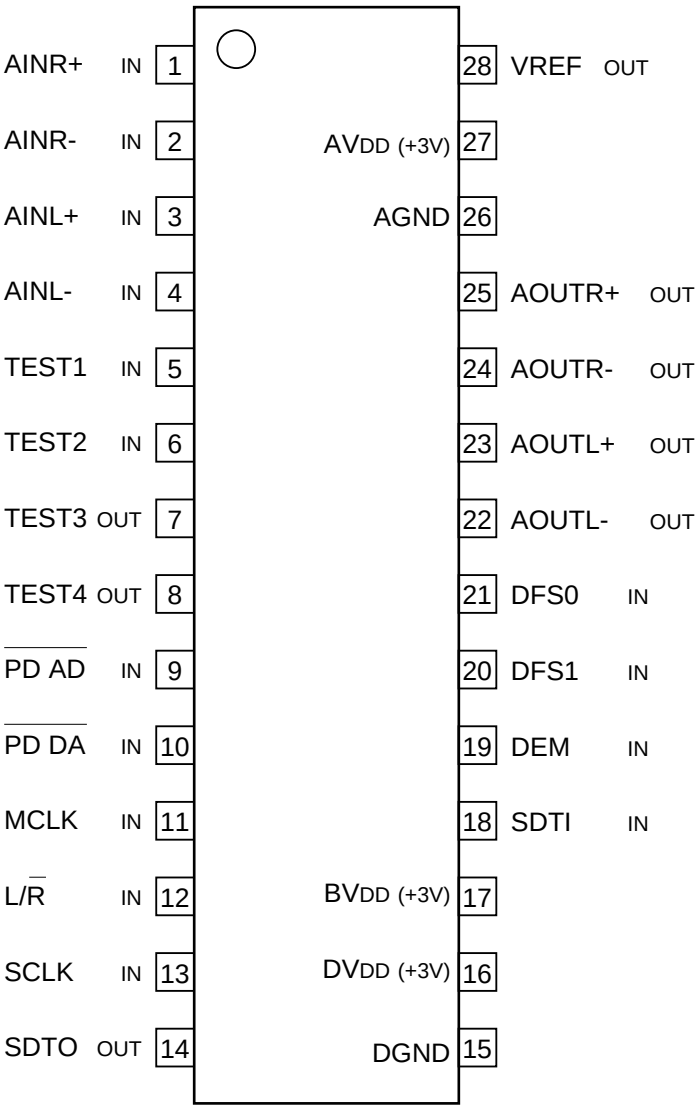
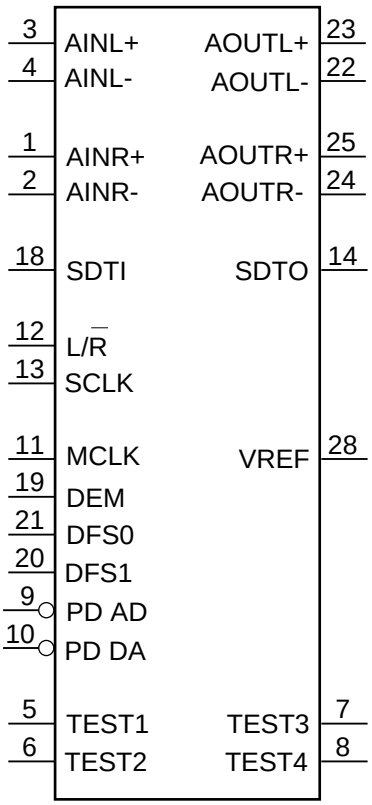
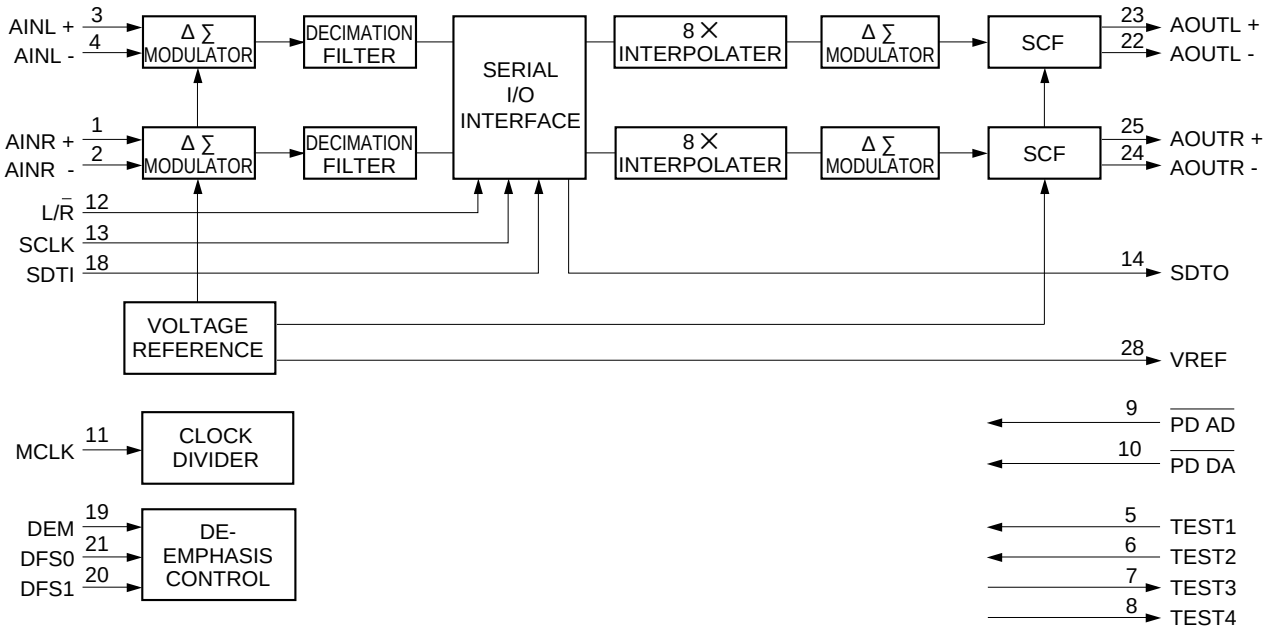
C-MOS 16-BIT A/D, D/A CONVERTER

—TOP VIEW—







INPUT

AINL +	;	CHANNEL L ANALOG POSITIVE INPUT
AINL -	;	CHANNEL L ANALOG NEGATIVE INPUT
AINR +	;	CHANNEL R ANALOG POSITIVE INPUT
AINR -	;	CHANNEL R ANALOG NEGATIVE INPUT
DEM	;	DE-EMPHASIS CONTROL
DFS0, DFS1	;	DE-ENPHASIS FREQUENCY SELECT
L / $\overline{R}$	;	INPUT/OUTPUT CHANNEL SELECT
MCLK	;	MASTER CLOCK
$\overline{PD\ AD}$	;	A/D CONVERTER POWER DOWN
$\overline{PD\ DA}$	;	D/A CONVERTER POWER DOWN
SCLK	;	SERIAL DATA CLOCK
SDTI	;	SERIAL DATA
TEST1, TEST2	;	TEST

OUTPUT

AOUTL +	;	CHANNEL L ANALOG POSITIVE OUTPUT
AOUTL -	;	CHANNEL L ANALOG NEGATIVE OUTPUT
AOUTR +	;	CHANNEL R ANALOG POSITIVE OUTPUT
AOUTR -	;	CHANNEL R ANALOG NEGATIVE OUTPUT
SDTO	;	SERIAL DATA
TEST3, TEST4	;	TEST
VREF	;	REFERENCE VOLTAGE